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10/526,421	03/01/2005	Jeroen Anton Johan Leijten	260670	3287

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EXAMINER	
FAHERTY, COREY S	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,421	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed on 07/31/2008.

2. Claims 1-13 and 15-17 are pending in the application and have been examined.

3. The 35 U.S.C. 112, second paragraph rejection of claims 11 and 17 made in the previous office action are withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), *at the time the application was filed*, had possession of the claimed invention. Claim 12 recites the limitation "being a VLIW processor and having a plurality of parallel issue slots of which only a single issue slot is used for implementing handling of nested interrupts." The examiner has argued that the traditional definition of a VLIW instruction is that each slot in the instruction is associated with a specific functional unit in the processor, and that it is therefore not clear how, in a traditional VLIW processor, a single issue slot could be capable of executing all instructions necessary for handling nested interrupts. Applicant has responded to this position by stating that a person who is skilled in the art could construct a VLIW processor from a parallel arrangement of full fledged CPUs. However, if this is indeed the intent of the

present claim language, then the claim does not meet the requirements of 35 U.S.C. 112, first paragraph because there is no teaching of such a system in the original teachings of the application. Furthermore, the development and design of such a system, based on the complexity of the art and the lack of direction provided by the inventor, would require undue experimentation. It should be noted that applicant has even pointed out how complex such a design would be in the arguments submitted 07/31/2008 [page 6, final paragraph].

6. Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), *at the time the application was filed*, had possession of the claimed invention. Claim 17 recites the limitation "wherein the controller means saves," ...", the state information of various processor state elements" ... "without requiring instruction bits, additional to a stack pointer, for addressing the snapshot buffer elements". Applicant has cited paragraph 19 of the publication of the application as supporting this limitation, which states: because "the snapshot buffer will maintain its own internal stack pointer, none of the above read/write commands will require a register address, as would have been required for standard random access register files." This disclosure teaches nothing regarding addressing snapshot buffer elements without using any instruction bits, but rather only teaches that certain commands do not require a register address. There is no mention in this teaching of addressing of snapshot buffer elements, with or without instruction bits. The claim is therefore not supported by the original disclosure.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 recites the limitation "being a VLIW processor and having a plurality of parallel issue slots of which only a single issue slot is used for implementing handling of nested interrupts." However, the traditional definition of a VLIW instruction is that each slot in the instruction is associated with a specific functional unit in the processor. It is therefore not clear how, in a traditional VLIW processor, a single issue slot could be capable of executing all instructions necessary for handling nested interrupts. The teachings of the present application fail to elaborate on how the VLIW achieves such capability, and the precise scope of the claim is therefore impossible to determine.

Applicant has argued that a person having skill in the art could construct a VLIW processor from a parallel arrangement of full fledged CPUs. The examiner respectfully points out that the design of a VLIW processor using multiple full CPUs is a significant design problem, and no such system is disclosed nor suggested in the teachings of the present application.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-3, 5-7, 9, 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen et al. (U.S. Patent 5,115,506), referenced from here forward as Cohen.

12. Regarding claims 1 and 13, Cohen discloses a data processor comprising:

one or more functional units [col. 3, lines 23-25; the processor can be of the 68000-family, all of which include a functional unit],

one or more register files [Fig. 1A],

a data memory having a multibit access port facility [Fig. 1A, memory stack],

a snapshot buffer which during the handling of an interrupt condition accommodates saving state information of various processor state elements in respective snapshot buffer elements [col. 8, lines 20-66; when an interrupt occurs, the register set that is used is switched so that the register data corresponding to each processing context is saved], and

a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility [Fig. 1A; col. 8, lines 33-66; when a nested interrupt occurs, the data present in the multiple

registers being used to execute the interrupt that is currently being handled is copied to a memory stack; col. 6, lines 12-18].

Cohen does not explicitly disclose that the system includes a processor pipeline nor that the saved state information is from a processor pipeline. However, the performance benefits of using a pipelined data path are well known and Cohen discloses saving data path state to memory in response to an interrupt condition [Fig. 1A; col. 8, lines 33-66]. It therefore would have been obvious to a person having ordinary skill in the art to save state information from an internal processor pipeline in response to an interrupt condition.

13. Regarding claim 2, Cohen discloses the data processor as claimed in Claim 1, wherein said controller means are arranged to retrieve the saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements upon completing the handling of the actual interrupt condition [col. 9, lines 50-65; when processing completes the handling of a nested interrupt, the processor un-stacks from memory stack back to the register set any data associated with execution of the handling of an interrupt that was interrupted].

14. Regarding claim 3, Cohen discloses the data processor as claimed in Claim 2, wherein said controller means are arranged to restore the retrieved saved state information of various processor state elements allowing said data processor to proceed with handling one of an earlier uncompleted interrupt or continuing a main thread of the processing [col. 10, lines 3-8; after interrupt processing completes, the processor switches back to using the original registers that were saved and continues normal operation].

15. Regarding claim 5, Cohen discloses the data processor as claimed in Claim 1, wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility [col. 8, lines 19-66; when an interrupt occurs, the data in registers corresponding to currently-executing interrupt handling code is saved to the stack memory; this data may be stored in different register sets, depending on the type of interrupt that is being handled; col. 8, lines 38-40; data may be stored from the prime registers to the stack; col. 8, lines 60-62; data may also be stored from the normal register set to the memory stack; Fig. 1A; the prime registers are separate from the normal register set, so the data that is written to the external memory stack must be multiplexed to determine which registers are being written from].

16. Regarding claim 6, Cohen discloses the data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility [col. 9, lines 36-54; the processor may unstack data from the memory stack to different register sets in the processor, making a multiplexing operation essential to determine which will be written to].

17. Regarding claim 7, Cohen discloses the data processor as claimed in Claim 1, wherein said data memory facility is operated as a stack [Fig. 1A; col. 7, line 14].

18. Regarding claim 9, Cohen discloses the data processor as claimed in claim 7, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring from said data memory facility [col. 9, lines 36-54; the processor may unstack data from the memory stack to

different register sets in the processor, making a multiplexing operation essential to determine which will be written to], wherein said snapshot buffer comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring to said data memory facility [col. 8, lines 19-66; when an interrupt occurs, the data in registers corresponding to currently-executing interrupt handling code is saved to the stack memory; this data may be stored in different register sets, depending on the type of interrupt that is being handled; col. 8, lines 38-40; data may be stored from the prime registers to the stack; col. 8, lines 60-62; data may also be stored from the normal register set to the memory stack; Fig. 1A; the prime registers are separate from the normal register set, so the data that is written to the external memory stack must be multiplexed to determine which registers are being written from], and wherein write and read operations in said stack are executed at mutually exclusive instants in time [col. 8, lines 38-40; information associated with a first executing interrupt handler is stored to the stack when the first interrupt handler is interrupted; col. 9, lines 50-54; later, when a second interrupt handler that handles the interrupt that interrupted the first interrupt handler completes execution, the information associated with the first executing interrupt handler is retrieved from the stack].

19. Regarding claim 15, Cohen does not explicitly disclose saving the processor state elements to the snapshot buffer in a single clock cycle. However, the concept and advantages of performing a data operation in a single clock cycle in a processing system are well known in the computer arts, and it therefore would have been obvious to one of ordinary skill in the art to do so.

20. Regarding claim 16, Cohen does not explicitly disclose restoring the processor state elements from the snapshot buffer in a single clock cycle. However, the concept and advantages of performing a data operation in a single clock cycle in a processing system are well known in the computer arts, and it therefore would have been obvious to one of ordinary skill in the art to do so.

21. Regarding claim 17, Cohen discloses the data processing facility of as claimed in Claim 1, wherein the controller means saves, upon occurrence of the subsequent interrupt condition during the handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility [Fig. 1A; col. 8, lines 33-66; when a nested interrupt occurs, the data present in the multiple registers being used to execute the interrupt that is currently being handled is copied to a memory stack].

Cohen does not explicitly disclose that the above operation is performed without requiring instruction bits, additional to the stack pointer, for addressing the snapshot buffer elements or the data memory facility. However, Cohen does teach that the data is written to the snapshot buffer and the data memory using a stack and a stack pointer [col. 3, lines 10-11; col. 8, lines 33-44], and that stack pointer is not a portion of an instruction. It therefore would have been obvious to address the snapshot buffer and the data memory using the stack pointer and not with instruction bits.

22. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Petolino, Jr. et al. (U.S. Patent 5,958,041), referenced from here forward as Petolino.

23. Regarding claim 4, Cohen discloses that the state to be saved during interrupt processing includes data that is associated with the currently executing code [col. 8, lines 38-40], but does not explicitly disclose that this data includes latency data of current operations.

Petolino discloses a processor in which each load instruction has an associated latency prediction bit that is used to predict the proper latency period between the issuance of a load instruction and the issuance of any dependent instructions [col. 4, lines 25-30]. The purpose of the bit is to minimize the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include instruction latency data of current operations in the state that is saved during interrupt handling in the system of Cohen because Cohen discloses saving any data that is associated with currently executing code in response to an interrupt [col. 8, lines 38-40] and Petolino discloses associating an instruction latency bit with each load instruction [col. 4, lines 25-30] for the purpose of minimizing the delay necessary for executing a load instruction and any dependent instructions in a processor [col. 4, lines 16-22, 59-67; col. 5, lines 1-8].

24. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 7 above, and further in view of Patterson et al. (*Computer Organization & Design: The Hardware/Software Interface*), referenced from here forward as Patterson.

25. Regarding claim 8, Cohen discloses the data processor as claimed in claim 7, wherein the processor has a stack pointer [Fig. 1B], but does not explicitly disclose that the stack pointer allows multiple stack positions per snapshot. However, Cohen does disclose that, during the

handling of an interrupt, an entire set of registers may be saved to the memory stack [col. 8, lines 40-44].

Patterson discloses a typical method for the handling of a stack memory structure in a processor [pages 134-135; Figure 3.10]. The method includes decrementing the stack pointer using a subtract instruction (sub) and using store instructions (*sw*) to push registers onto the stack. Because multiple registers are pushed onto the stack, the value of the stack pointer is decremented by a value three times the size of each register. In this way, the multiple registers are pushed onto the stack at different stack locations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the stack pointer of Cohen allow multiple stack positions per snapshot because Cohen discloses that a single snapshot includes multiple registers [col. 8, lines 40-44] and Patterson discloses a typical method for handling a memory stack in which each register that is pushed onto the stack has its own stack location [pages 134-135; Figure 3.10]. Furthermore, allowing each register to have its own stack location gives the processor more versatility in determining which registers will be saved on the stack, potentially decreasing the processing time required to perform the save operation.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Nguyen et al. (U.S. Patent 5,448,705), referenced from here forward as Nguyen.

27. Regarding claim 10, Cohen does not explicitly disclose that the snapshot buffer comprises shadow flipflops for storing snapshot information.

Nguyen discloses a method for handling traps in a processor in which, when a trap is encountered, a number of shadow registers are shifted to the foreground to be used by the trap handling routine and the corresponding foreground registers are shifted into the background to be saved as shadow registers [col. 3, lines 54-64]. The purpose of using shadow registers to construct a snapshot buffer in the processor is so the trap handler has a set of registers immediately available for use without any need to be concerned about destroying data needed for the main instruction stream [col. 3, lines 61-64].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use shadow flipflops to store snapshot information in the processor of Cohen because Nguyen discloses using shadow registers to hold snapshot information during a trap [col. 3, lines 54-64] and teaches that doing so allows the trap handler to immediately access registers without being concerned about destroying data needed for the main instruction stream, because that data is stored in the new shadow registers [col. 3, lines 54-64].

28. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Lang et al. (*Individual Flip-Flops with Gated Clocks for Low Power Datapaths*), referenced from here forward as Lang.

29. Regarding claim 11, Cohen discloses the data processor as claimed in claim 1, wherein the processor has a stack pointer [Fig. 1B], but does not explicitly disclose that the flipflops comprising the stack pointer are clocked only during stack pointer updates.

Lang discloses a method for operating flipflops in which the flipflops are only clocked when the flipflop must change [section 1, paragraph 3]. The purpose of doing this is to reduce the energy that is consumed by the clock circuits internal to the flipflop [section 1, paragraph 3].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clock the flipflops comprising the stack pointer in Cohen only during stack pointer updates because Lang discloses a technique in which flipflops are clocked only when the flipflop must change values [section 1, paragraph 3] and teaches that using this technique reduces the energy that is consumed by the clock circuits internal to the flipflop [section 1, paragraph 3].

30. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Kleiman (U.S. Patent 5,515,538).

31. Regarding claim 12, Cohen discloses the data processor as claimed in claim 1, but does not explicitly disclose that it is a VLIW processor nor that it has a plurality of issue slots and that only a single issue slot handles the processing of nested interrupts. However, a person having ordinary skill in the art will recognize that the interrupt handling techniques of Cohen are applicable to a VLIW processor and will have the same benefits. Furthermore, Kleiman discloses a system in which dedicated hardware is used for interrupt handling. Specifically, in the system of Kleiman, only special kernel threads are used to perform interrupt handling [col. 7, lines 60 – col. 8, line 17; col. 9, lines 10-23; col. 10, lines 16-17]. By using dedicated thread contexts to perform the interrupt handling, the system of Kleiman reduces processing overhead as compared to a system that handles interrupts using any thread context because not all thread contexts will need to be capable of performing interrupt handling operations. A person having ordinary skill in the art will recognize that such reasoning can be applied to VLIW processing slots as well. Using a single VLIW slot to handle interrupts reduces processing overhead because the other slots will not have to be capable of performing such processing. Such operation would therefore have been obvious to a person having ordinary skill in the art.

Response to Arguments

32. Applicant's arguments filed 07/31/2008 have been fully considered but they are not persuasive. Applicant argues that certain elements of Cohen do not constitute elements that are part of an "internal processor pipeline". However, this term is very broad and the examiner must interpret it accordingly. More specifically, the term "internal processor pipeline" may refer to virtually any portion of a modern processing system. Applicant's argument is apparently relying on a very specific definition of this term. However, for such a definition to be considered, it must be explicitly recited in the claim language. The argument is therefore not persuasive. Furthermore, as stated in both the previous and present rejections, the use of a pipeline would have been obvious to a person having skill in the art. Applicant has made no argument to overcome this position and the rejection is therefore maintained.

Conclusion

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
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